IN THE SPECIFICATION

The following paragraphs are rewritten pursuant to 37 C.F.R. §1.121.

1. Replace the paragraph beginning at page 8, line 9 of the specification with the following paragraph:

Figure 2 illustrates that the modulation of the supply voltage signal V_{dd} according to the invention corresponds with the modulated clock frequency. When the supply voltage signal V_{dd} is at its highest level, the clock frequency C is also [[that]] at its highest level. On the other hand, when the supply voltage V_{dd} is lowest, the clock frequency C is also at its lowest level. This relationship between the modulated supply voltage V_{dd} and modulated clock frequency C produces several benefits. First, the modulated clock frequency causes circuit 10 to produce a lower average EMI emission energy over a given operating period. Second, the higher performance exhibited by circuit 10 at the higher supply voltage will support the higher clock frequency at the appropriate time in the spread spectrum cycle, and the lower voltage supplied during the slower clock frequency will help keep the power dissipation in the circuit down to acceptable levels.

Respectfully submitted,

The Culbertson Group, P.C.

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CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, (Fax No. 703-872-9306) on July 7, 2005.

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